Study of the factors influencing power consumption of FPGA-based designs

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The paper presents results from the study of power consumption of basic circuit designs on FPGA with different VHDL descriptions, different elaborated and synthesized structures and realized on different devices. The study is performed for 4 different VHDL descriptions (behavioral and structural) of 4-bit comparator and realizations on Xilinx FPGA circuits from the families Artix-7, Zynq 7000 all programmable System-on-a-chip (SoC) or on the Xilinx board Zedboard. The Xilinx software Vivado 2014 is used and the function Power report is implemented for power consumption study. Power consumption is sensitive to factors enumerated. For the 4-bit comparator studied it goes to 29% increase of dynamic power for structural VHDL description and it shows that the low-power design on FPGA should start with the low power design of very basic structures as combinatorial logic circuits.

Keywords – 4-bit comparator, FPGA, Power consumption, VHDL code

Изследване на факторите влияещи на консумацията на проекти, реализирани върху програмируеми схеми FPGA (Галя Маринова, Здравка Чобанова). *Статията представя резултати от изследването на консумираната мощност на схемни проекти, реализирани върху програмируеми схеми FPGA, основани на различни описания на VHDL кода (поведенчески и структурни), различни логически и синтезирани структури, и реализирани върху различни устройства. Изследването е направено за 4 различни описания на VHDL кода на 4-битов компаратор и последващата им реализация върху Xilinx FPGA схеми от фамилиите Artix-7, Zynq 7000 напълно програмируеми системи-върху чип (SoC) или върху платката на Xilinx Zedboard. Използван е софтуерът за цифрово проектиране Vivado 2014 на Xilinx, а резултатите за изследваната мощност на всяка проектна реализация са получени с опцията Power report. Изследването показва, че консумираната мощност зависи от изброените по-горе фактори. При структурно описание на VHDL на 4-битовия компаратор се получава до 29% нарастване на изразходваната динамична мощност в сравнение с поведенческото описание, следователно проектирането върху FPGA за ниска консумация би следвало да започне с проектирането за ниска консумация на базисните схемни структури, например комбинационните логически схеми.*

1. Introduction

The paper presents the results of a research, part of a project in Technical University-Sofia on design technics for green telecommunications. An overview on green communications is presented in [1] and some results of power consumption power estimation on FPGA and USRP-based platforms are presented in [2]. As noticed in [5] FPGA are 12 times less power efficient than ASICs because of the large number of transistors per logic function, necessary for programming. Static power in CMOS circuits is the power consumed when the circuit is not active, dynamic power is the power consumed when the logic toggles. Dynamic power is predominant in CMOS based devices - CPLD, FPGA, digital ASICs and it's a sum of switching power due to charging and discharging of output capacitance and short circuit power due to non-zero rise/fall times. It can be calculated as [4]:

$$P_{dyn} = \left(\frac{1}{2}C.V^2 + Q_{short-circuit}V\right).f \,, \quad (1)$$

where P_{dyn} - dynamic power C – load capacitance, V-power supply voltage, f - switching frequency, $Q_{short-circuit}$ - short-circuit charge.

The average power consumption in an FPGA can be calculated as:

(2) $$P_{avg} = \frac{1}{2}\sum_{i=1}^{n} C_i f_i V^2,$$

where P_{avg} - average value of dynamic power dissipation, C_i – capacitance of the net i, V-power supply voltage, f_i - average switching frequency, n-number of nets.

Recently different studies are performed in order to model and reduce power consumption in FPGAs, as shown in the overview from [3]. Dynamic power consumption is architecture dependent [6], data dependent, hardware description language (HDL) code dependent [5]. Different techniques are proposed to reduce dynamic power on clock scheme, logic power, RAM power, I/O power by optimal selection of adder and multiplier blocks, counters, FSMs, general glitch reduction techniques on logic, logic partitioning rearranging, etc.

Authors of [5] study 2 HDL codes of a 4-bit unsigned up counter with asynchronous clear and clock enable on Xilinx Virtex-6 FPGA - the first code maps the clock enable signal to LUTs and the second maps it to the control ports and they obtain 6% power consumption reduction in the first design. The study in the current paper is focused on the influence of VHDL codes of combinatorial circuits' designs, implemented on FPGAs, on their power consumption and the impact of FPGA device on the power consumption of the design. The design studied is a 4-bit comparator and the simulator used is Vivado 2014. It is selected because it is realized with XOR circuits, which have significant power consumption [7]. The FPGA implementations and devices are studied, because they are widely used for communication systems [8]. The size of 4-bit was selected for comparison of behavioral and structural VHDL descriptions.

2. Study of the VHDL description influence on power consumption of FPGA-based designs

Four different VHDL descriptions of a 4-bit comparator are studied for power consumption in this section. The entities (ekv1, ekv2, ekv3, ekv4) of the 4-bit comparator, described in VHDL are identical for the 4 different architectures as shown on Fig.1.

```
entity ekv1 is
   Port ( a : in STD_LOGIC_VECTOR (0 to 3);
          b : in STD_LOGIC_VECTOR (0 to 3);
          a_eq_b : out bit);
end ekv1;
```

Fig.1. Entity of the 4-bit comparator.

Table 1 shows the 4 different VHDL codes of the 4 different architectures for the 4-bit comparator, implemented on ZedBoard with circuit Zynq™-7000 SoC XC7Z020-CLG484-1 [10]. The behavioural simulation of the designs is presented on Fig. 2.

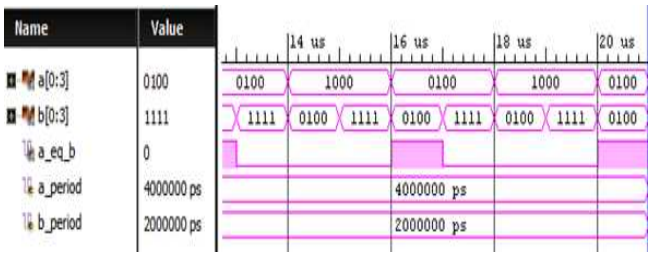


Fig.2. Simulation of 4-bit comparator in Vivado 2014.

For each description elaborated and synthesized designs are obtained with the options:

Implemented design > Report power

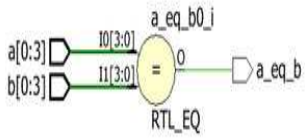
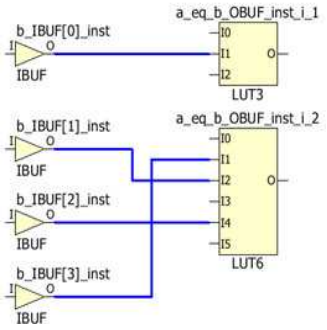
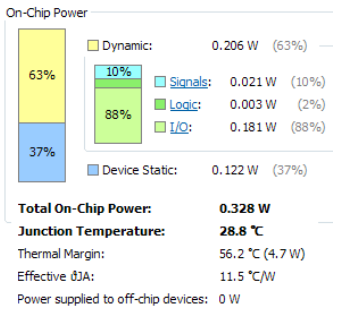
in VIVADO 2014, as shown in Table 1. The numbers of cells and nets differ for each description: (1 Cell, 9 Nets), (8 Cells, 16 Nets), (1 Cell, 9 Nets), (5 Cells, 13 Nets) for the elaborated designs and (6 Cells, 4 Nets), (11 Cells, 19 Nets), (11 Cells, 19 Nets), (11 Cells, 19 Nets) for the synthesized designs. The basic elements of the synthesized designs are 1 LUT3 and 1 LUT6 and different buffers. The first 3 VHDL descriptions are behavioral and the forth description is structural. Behavioral descriptions in VHDL are based on logical equations and truth tables and structural descriptions are based on schematic description with components and connections between them. Table 3 presents the on-chip power consumption of designs from Table 1. The on-chip power values for the first 3 descriptions are very close and they have similar structure for total power, dynamic power, static power, power dissipation in signals, logic and I/Os. The structural description leads to 29% larger total on-chip power consumption and different repartition of the on-chip power 71% dynamic power/ 29% static power compared to 63% dynamic power/ 37% static power in the 3 designs with behavioral architectures. Power dissipation in Logics stays almost invariant in all 4 designs - with a value of 0.03-0.04 W or 2% of the total on-chip power for behavioral descriptions and 1% for structural description. I/O power increases with 13% in the design with structural description. The largest difference is in the values of power for signals. The increase for structural description is 4.29 times the power for behavioral descriptions. The static power consumption stays almost invariant - 0.122-0.123 W and it's 37% of total on-chip power for

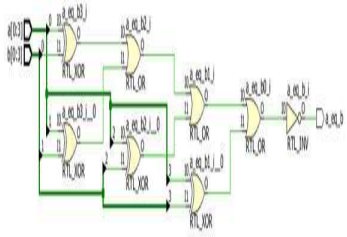
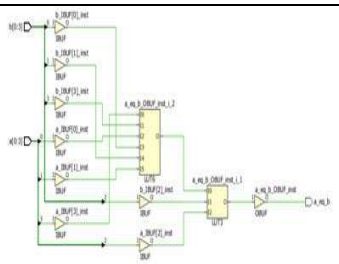
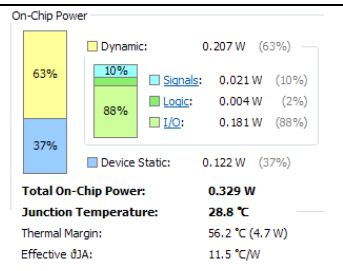
behavioral descriptions and 29% of total on-chip power for structural description. This study shows that the VHDL description of a design - behavioral or structural, influences the dynamic power consumption of the corresponding design and almost not the static power consumption. The most influenced elements of power are signals and I/Os.

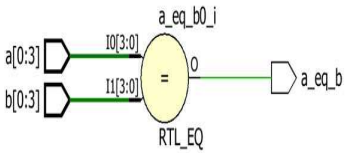
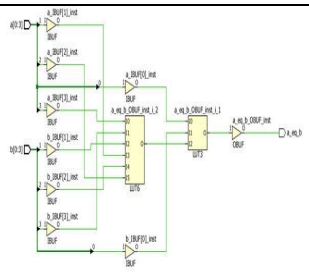
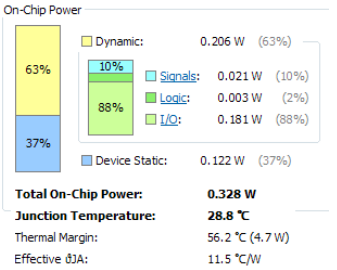
Table 1

Power consumption of a 4-bit comparator project on XILINX FPGA, designed from different VHDL descriptions

VHDL code	Elaborated design	Synthesized design	On-chip Power

architecture Behavioral of ekv1 is
begin
process (a,b)
begin
if a=b then
a_eq_b<='1';
else
a_eq_b<='0';
end if;
end process;
end Behavioral;
	
	1 Cell 9 Nets
		
		6 Cells 4 Nets
			

architecture Behavioral of ekv2 is
begin
a_eq_b<=
not((a(0)xor b(0))or (a(1)xor b(1))or (a(2)xor b(2))or (a(3)xor b(3)));
end Behavioral;
	
	8 Cells 16 Nets
		
		11 Cells 19 Nets
			

architecture Behavioral of ekv3 is begin a_eq_b<= '1' when (a=b) else '0'; end Behavioral;	 1 Cell 9 Nets	 11 Cells 19 Nets	

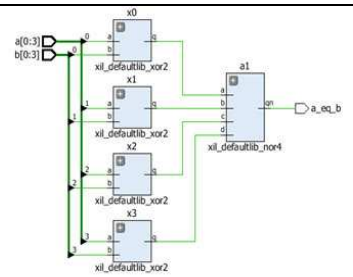
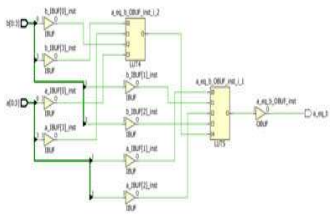
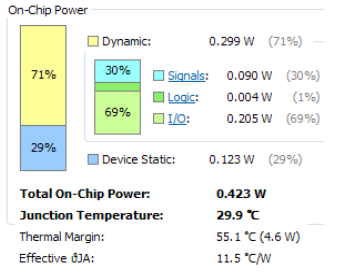
architecture Structural of ekv4 is
component xor2
port (a,b:in std_logic;
q: out std_logic);
end component;
component nor4
port (a,b,c,d: in std_logic;
qn:out std_logic);
end component;
signal c:STD_LOGIC_VECTOR (0 to 3);
begin
x0: xor2 port map(a(0),b(0),c(0));
x1: xor2 port map(a(1),b(1),c(1));
x2: xor2 port map(a(2),b(2),c(2));
x3: xor2 port map(a(3),b(3),c(3));
a1: nor4 port map (c(0),c(1),c(2),c(3), a_eq_b);
end Structural;
	
	5 Cells 13 Nets
		
		11 Cells 19 Nets
			

Table 2

Power consumption estimation of a design implemented on different XILINX FPGAs

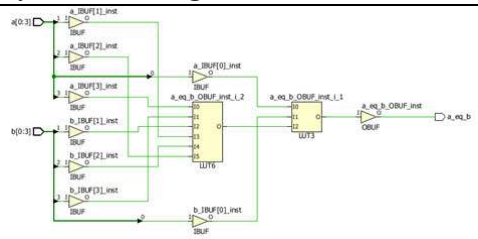
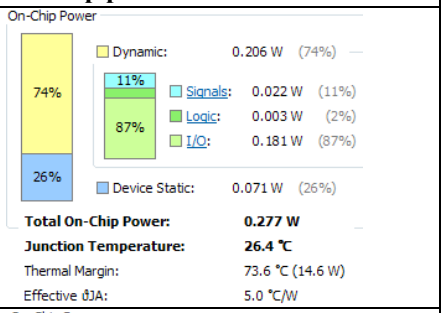
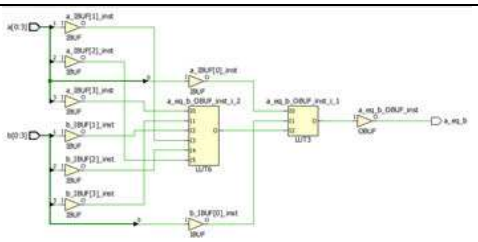
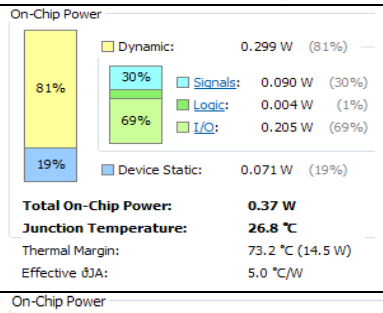
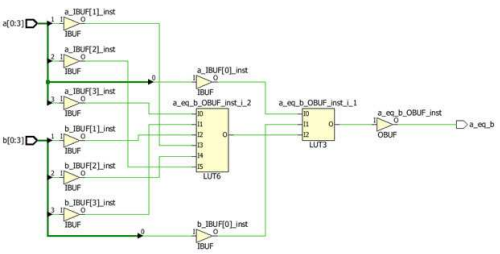
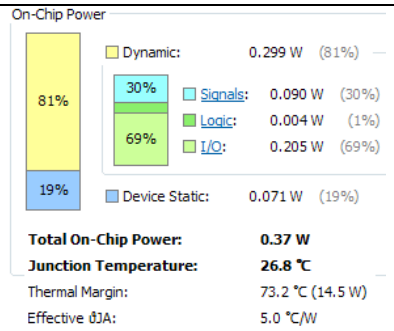
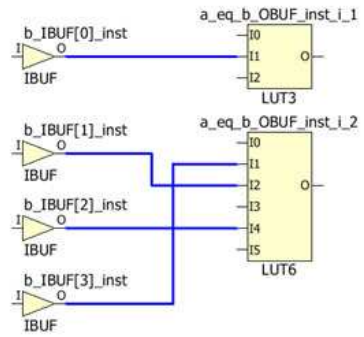
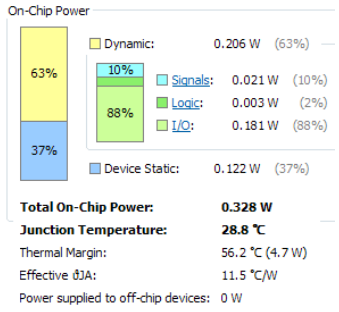
FPGA	Synthesized design	On-chip power
xa7a35tcpg236-2I (active), Family Artix-7		
xc7a35tcpg236-3 (active) Family Artix-7		
xc7z010clg225-3 (active), Family Zynq 7000 all programmable SoC		
ZedBoard with circuit Zynq™-7000 SoC XC7Z020-CLG484-1		

Table 3

On-chip Power consumption in [W] of designs from Table 1

VHDL Code	Total On-chip Power	Static Power	Dynamic Power	Power in Signals	Power in Logic	Power in I/O
Ekv1	0.328	0.122	0.206	0.021	0.003	0.181
Ekv2	0.329	0.122	0.207	0.021	0.004	0.181
Ekv4	0.328	0.122	0.205	0.021	0.003	0.181
Ekv4	0.423	0.123	0.299	0.090	0.004	0.205

Table 4

On-chip Power consumption in [W] of designs in Table 2

FPGA	Total On-chip Power	Static Power	Dynamic Power	Power in Signals	Power in Logic	Power in I/O
xa7a35tcpg236-2I	0.277	0.071	0.206	0.022	0.003	0.181
xc7a35tcpg236-3	0.37	0.071	0.299	0.090	0.004	0.205
xc7z010clg225-3	0.37	0.071	0.299	0.090	0.004	0.205
ZedBoard	0.328	0.122	0.206	0.021	0.03	0.181

The power consumption of logic is slightly affected by the VHDL description. The maximal delay from input to output ports in the 3 designs with behavioral description is 7.279 ns and for the design with structural description, the value is slightly higher 7.411 ns. The results show that at early stage of design, it is important to select a low power VHDL description for the basic combinatorial circuits in order to help the low power design of a more complicated system on FPGA.

3. Study on the influence of device selection on the power consumption of FPGA-based design

In this section the influence of device selected for a design is studied. The 4-bit comparator ekv1 with the first behavioural description from Table 1 is implemented on 4 different Xilinx FPGAs:2 from the family Artix-7 [9]: xa7a35tcpg236-2I and xc7a35tcpg236-3 and 2 from the family Zynq™-7000 - the first one is xc7z010clg225-3 and the second one is XC7Z020-CLG484-1 on Zedboard [10].

The VHDL description of the architecture used is:

```
architecture Behavioral of ekv1 is
begin
    comp: process (a,b)
    begin
    if a=b then a_eq_b<='1';
    else a_eq_b<='0'; end if;
end process comp;
end Behavioral;
```

Table 2 presents the synthesized designs for each device and the data for powers consumption. Table 4 presents the values for on-chip power consumption of designs in Table 2.

The total on-chip power is lower for the device xa7a35tcpg236-2I - 0.277 W and it's higher for xc7a35tcpg236-3 and xc7z010clg225-3 - 0.37 W, which results in 34% difference.

All 4 implementations have different repartitions between dynamic and static power:74% - 26% for xa7a35tcpg236-2I , 81% - 19% for xc7a35tcpg236-3 and xc7z010clg225-3, 63%-37% for Zedboard. Static power for the devices xa7a35tcpg236-2I, xc7a35tcpg236-3 and xc7z010clg225-3 is identical - 0.071 W, but for Zedboard it's 0.122 W, which is 72% larger.

Dynamic power in xa7a35tcpg236-2I and Zedboard is 0.206 W and in xc7a35tcpg236-3 and xc7z010clg225-3 it's 0.299 W, which is 45% larger.

Dynamic power in Logic is almost identical in 4 devices 0.03-0.4 W (1-2%).

Power in I/Os for xa7a35tcpg236-2I and Zedboard is 0.181 W and in xc7a35tcpg236-3 and xc7z010clg225-3 it's 0.205 W, which represents 13% increase.

Power consumption in signals has the most significant increase - for xc7a35tcpg236-3 and xc7z010clg225-3 the increase is 4.29 times, compared to the power consumption in signals for xa7a35tcpg236-2I and Zedboard implementations.

These data show that the selection of the device for implementation of a design has a serious impact on its power consumption, both dynamic and static, and it has to be considered. As in previous section, the largest differences are in power consumption for signals and there are very slight or null difference for power consumption in logic.

4. Conclusion

The study performed on the impact of different VHDL description (and corresponding elaborated and synthesized schematics) of a circuit design, show that the description might strongly increase the power consumption. The design of a 4-bit comparator with structural description, implemented on Zedboard, shows 29% larger consumption compared to the 3 behavioral descriptions of the same circuit. Static power consumption of the 4-bit comparator is almost not affected by the VHDL description. Structural description is very intuitive for the designer but it's not optimized in terms of complexity in implementation. This explains the higher power consumption in structurally described designs. Structural description leads to slightly higher maximal port to port delay.

The repartition of power consumption depends both from the VHDL description and from the device on which the 4-bit comparator is implemented. The power consumption in signals is the most sensitive to different VHDL descriptions and to different devices. It goes to 4.29 times of difference. Dynamic power consumption for logic seems the least sensitive to VHDL description code and to device selection. Power in I/Os varies about 13% from the VHDL code description and device selection.

The results from this study show that even for combinatorial circuits the type of VHDL code description has important influence on power consumption. Structural description might increase the power consumption. So, when a more complicated design is planned, the basic structures should be designed initially for low power, in order to achieve lower power consumption of the final complex design. On the other side the type of device selected for a

design is also influencing the power consumption, so it should be considered at the early stage of the design, when basic structures are described and tested.

Further research is foreseen on clock-driven designs as random bit and number generators.

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