A general concept and implementation of a DSP-based QAM digital modulator

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The versatility of a Digital Signal Processor (DSP) can be used to implement easily various Quadrature Amplitude Modulation (QAM) tasks on a prototype board interconnected to the ADSP21061 EZ-KIT LITE DSP evaluation system extension ports. The article describes the allocation of the different subtasks associated with the digital modulation to the DSP hardware and to the extension board respectively. The prototype board consists of two high speed Digital-to-Analog Converters for the I- and Q-components of the QAM signal, a dedicated QAM modulator chip working in the analog domain and a RF local oscillator chip to supply the carrier signal to the modulator. The different constellation diagrams the proposed modulator can carry out are synthesized by the DSP hardware through symbol remapping look-up tables. The complete hardware circuit diagram of the prototype board DM9753 is presented and discussed in the article and the future investigation and experimental measurement works to be performed on the digital modulator proposal are outlined.

Обща концепция и реализация на базиран на цифров сигнален процесор квадратурно-амплитуден (QAM) модулатор (Емил Е. Владков). *Гъвкавостта на цифровите сигнални процесори (DSP) може да бъде използвана за лесно осъществяване на различни задачи, свързани с квадратурно-амплитудната модулация (QAM), посредством прототипна система, свързана към разширителните портове на ADSP21061 EZ-KIT LITE DSP развойната система. Статията описва разпределението на различните подзадачи, свързани с цифровата модулация, към апаратното осигуряване на цифровия сигнален процесор и към разширителната платка съответно. Прототипната система се състои от два високоскоростни цифрово-аналогови преобразувателя за I- и Q-компонентата на QAM сигнала, специализирана интегрална схема, съществяваща QAM модулатицята в аналоговата област, и интегрална схема на радиочестотен локален осцилатор, осигуряващ носещия сигнал на модулатора. Различните констелационни диаграми, които предложеният модулатор може да осъществява, се синтезират от апаратното осигуряване на DSP посредством таблично представяне на координатите на отделните символи данни. Представена и дискутирана е пълната схемна реализация на прототипната система DM9753 и са очертани задачите на бъдещата изследователска и експериментална измервателна работа по предложения цифров модулатор.*

I. Introduction

A state of the art versatile digital modulator is a piece of equipment, which not only serves various purposes at the test bench but is also indispensable for the in-depth understanding of this widespread new technology – digital modulation. For engineering students not familiar with high-speed digital modulation the proposed concept and design is an opportunity to draw the curtains in this field, of course in combination with the study of various excellent books on digital communications [1]. For engineers dealing with the various aspects of QAM, QPSK and the like in their everyday professional life the proposed concept will offer a new versatile (and this is perhaps the most important aspect in this context) device for generating digital sequences, which can be programmed by themselves to suit their individual needs. The presented idea is to be tested in a future work with a custom build evaluation board wired to the ADSP-21061 floating-point digital signal processor (DSP) evaluation system. The combined DSP-based digital modulator will also have the

capability to be interfaced to various sources of digital data for transmission on a RF-channel, provided the interface specifications of the board are met.

II. Main principles and application areas of digital modulation

The term "digital modulation" is usually used to describe the process of modulation of an analog carrier by digital data, where the bit combination directly determines some of the characteristics of an analog signal – the amplitude, the frequency, the phase or a combination of them. The simple forms of digital modulation are these which modify only one of the parameters of the analog signal – and these are the Amplitude-Shift-Keying (ASK), the Frequency-Shift-Keying (FSK) and the Phase-Shift-Keying (PSK, QPSK). The more sophisticated techniques influence both amplitude and phase to transmit more bits in one state of the signal (or in one symbol, which is the other term for the "state" of the signal). Typical examples of such sophisticated modulation methods are the various kinds of Quadrature Amplitude Modulation (QAM) – QAM-16, QAM-32, QAM-64, QAM-256 and so on. The number after the QAM abbreviation represents the number of the separate states the signal can have. As each state is unique a unique bit pattern can be transmitted with this "symbol". The more the symbols the more the bits in the bit pattern that can be transmitted. So in QAM-16 there are 16 symbols, so only 4 bits can be transmitted, in QAM-64 the number of bits is 6 and in QAM-256 it is a whole byte (8 bits) that can be transmitted at once. It is obvious that these digital modulation techniques can be used to transmit high bit rates on narrowband channels (as the bandwidth required is determined by the symbol change rate and not the number of bits carried by each symbol). So QAM is widely used in digital microwave radios, where bit rates up to 155Mbps can be easily achieved (the STS-3 SONET hierarchy signal) on a channel with a bandwidth of only 19.4MHz (broadband – modulated carrier and not baseband) [2].

Other application areas of QAM are the widespread WiFi 802.11 a,g,n wireless networking standards [3] and the current generation digital cable systems [4]. The digital TV downstream signal for example makes use of QAM-64 and QAM-256 to carry MPEG packets to the cable subscriber. There are different standards for digital cable TV in the different countries – they differ mainly in the error-correction techniques employed. In North America the digital cable standard is the ITU-T/J.83B, Annex B, in Europe it is the DVB-C, Annex A, in Japan it is the ITU-T/J.83B, Annex C. A simplified illustration of the various stages of a QAM digital modulator for cable TV is represented in Fig. 1. It is obvious that there are many other functions besides the bits-to-QAM-symbols mapping, which should be performed by the commercial DVB-C modulator. The versatile modulator proposal described in this article performs some of the depicted functions too (shown in gray in the Figure), and because the device is programmable many other functions can be easily added by the user. The design proposed not only remaps data according to the constellation diagrams used, but also shall perform Trellis Coded Modulation (TCM) to provide a better error performance for a given channel signal-to-noise ratio. A Root Raised Cosine Filtering for better Inter-Symbol-Interference (ISI) will be included in the design too. The modulation of a carrier with the QAM-modulated baseband signal can be performed through a dedicated RF-up-converter hardware (IC). The processing of the serial video ASI interface and the MPEG-2 framing are not dealt with as in the case of a versatile evaluation board the information source for the data to be transmitted can not be restricted to video data only. Some of the data processing in the design proposed is performed somewhat differently compared to the block diagram in Fig. 1 – the main differences arising from the migration of some of the functions from the analog to the digital domain and vice versa – the general principle remains the same.

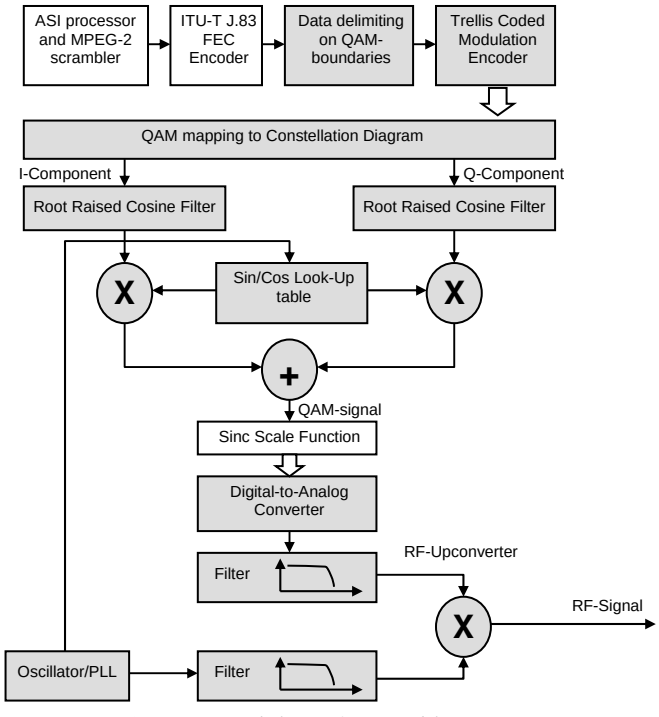

Fig.1. QAM modulator for a cable TV system.

III. Digital Modulation with a DSP

The general block diagram of the proposed DSP-based digital modulator is shown in Fig. 2. The most manifest difference to the cable system modulator presented in Fig. 1 is that the downright quadrature modulation of both component signals (I and Q) on both carriers, one in phase and one in quadrature, is performed in hardware by a dedicated QAM-modulator chip AD8345 and not by the digital signal processor [5]. The DSP resides on the ADSP21061 EZ-KIT LITE evaluation board, provided by Analog Devices [6]. For communication and downloading the firmware programs to the DSP-board to accomplish debugging and measurement tasks the evaluation copy of the Integrated Design Environment (IDE) VisualDSP++, which comes bundled with the EZ-KIT LITE, is used. VisualDSP++ allows the user to write assembly or C-language programs, specify the architecture of the target system in a Linker Description File (LDF), compile and link the programs, simulate their behaviour and plot expected and real world result and finally download the programs to the target hardware (the EZ-KIT LITE) [7]. Complete control over the running program on the DSP through the integrated debugging features is provided. The firmware code of the QAM modulator in assembly language for the ADSP-21xxx family of signal processors will be prepared and compiled in this way. The J1 and J6 2x20 and 2x25 header connectors on the EZ-KIT LITE board are used to interface the evaluation board to the daughter modulator board through ribbon cables as shown in Fig. 2. They carry all necessary data port and clock signals to supply the modulator with the digital I- and Q-signals. As the EZ-KIT LITE board comes with unpopulated header extension connectors they have to be soldered in place. The data bus is 48-bit wide and is divided in 4x12-bit parallel words. Two 12-bit Digital-to-Analog Converters (DACs - AD9753 [8]) on the modulator board perform the conversion from the digital to the analogue domain. As with every DAC the outputs of the converters are low-pass filtered with dedicated 51MHz filters. The smoothed I- and Q-components are fed to the AD8345 modulator, which is supplied with a local oscillator RF-signal generated by the RF MAX2620 oscillator [9]. The output of the board is a QAM-modulated RF carrier with the frequency of 433MHz, but a 900MHz version should work equally well on the same hardware. Actually every frequency between 250MHz and 1GHz can be used for the RF-carrier signal [5]. A more detailed discussion on the hardware schematics will follow in the hardware implementation section.

IV. QAM Constellation Diagrams

The Quadrature Amplitude Modulation (QAM) manipulates both amplitude and phase, so the usual approach to deal with it is to represent every state by a rotating vector in the so-called I-Q plane. This representation can be achieved by combining two carriers as stated earlier – one in-phase (the I-carrier) and one in-quadrature (the Q-carrier). So the constellation diagram is actually a representation of two amplitude modulation processes performed on the two carriers and this amplitude modulation can have only discrete values. The typical QAM display

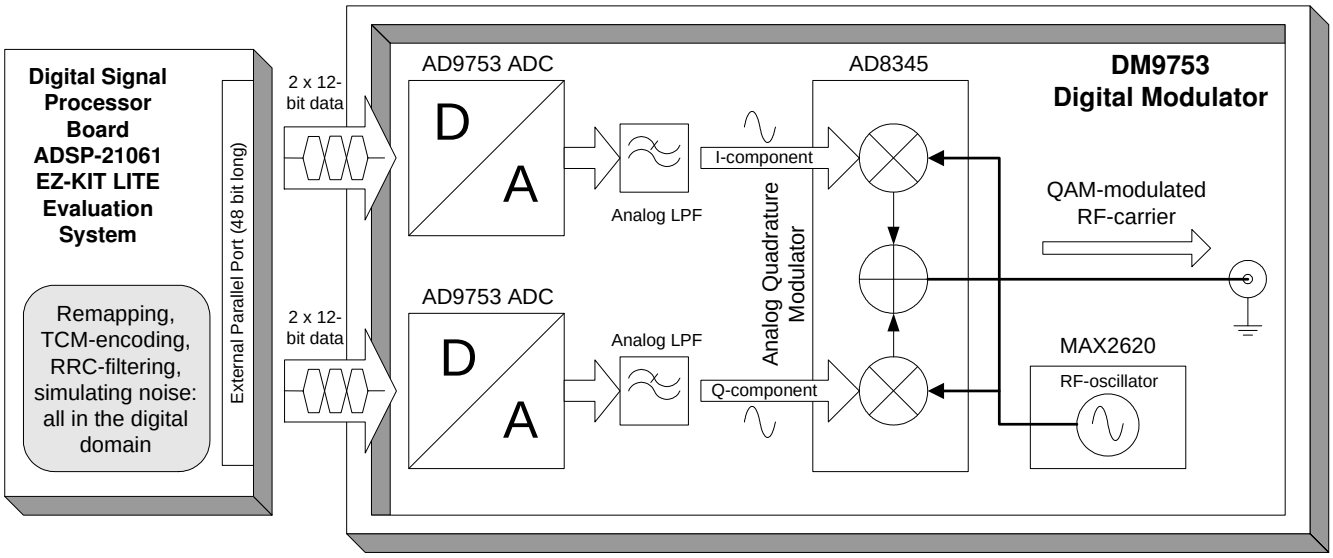

Fig.2 Block diagram of the DSP-based Digital Modulator concept.

consists of equally (or not equally) spaced points, every point representing one symbol transmitted at any given time [10]. The neighbour states usually differ in only one bit – this is the so-called Gray-coding. The main goal of implementing Gray-coding is better error performance – due to phase noise or bad signal-to-noise ratio on the channel one state can be interpreted in error as another (near the original one) state at the receiver. Messing up neighbouring states leads to only one-bit errors in this coding case, which can be easily corrected through other methods. Three

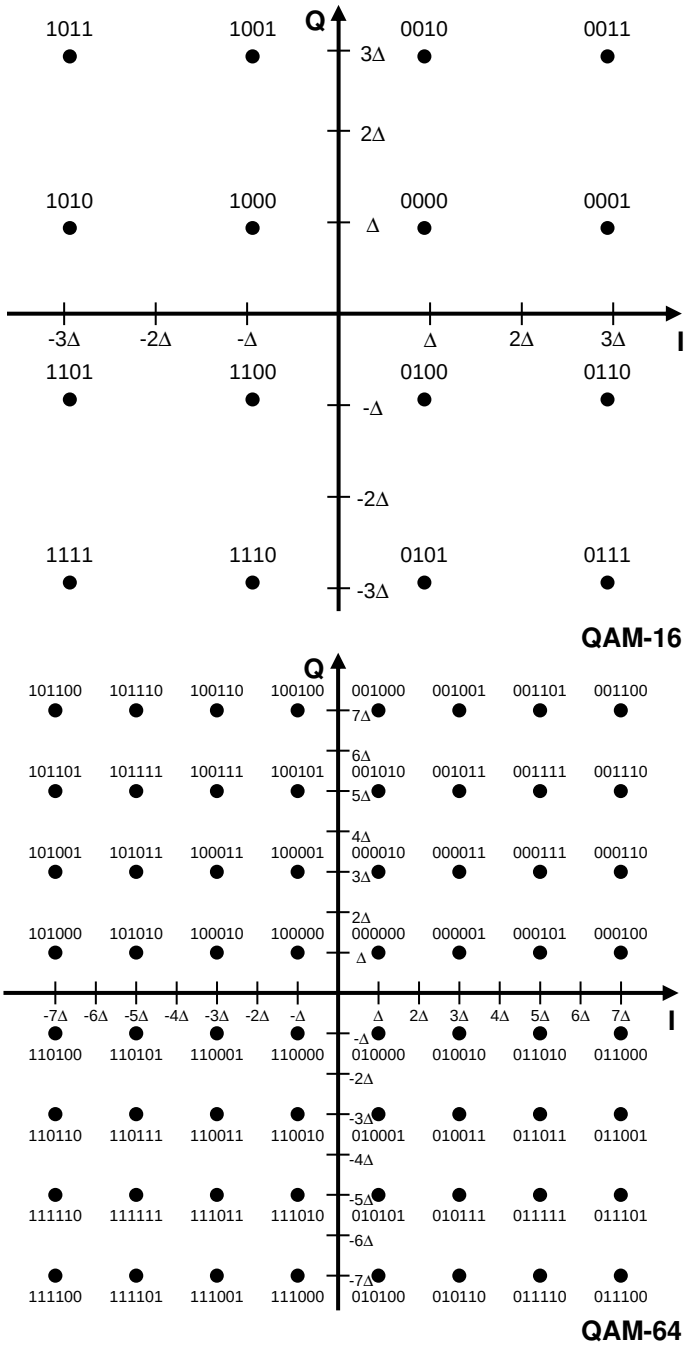

Fig.3. Constellation Diagrams for QAM-16 and QAM-64.

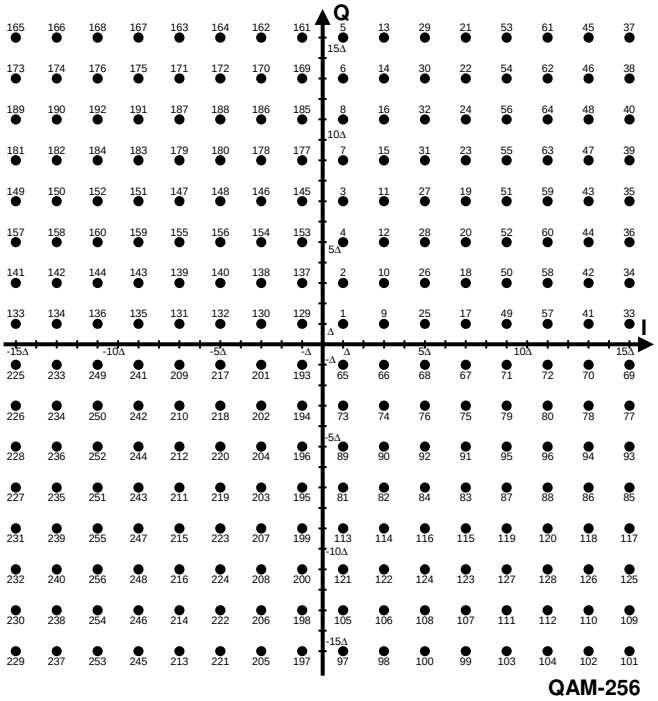

Fig.4. Constellation Diagram for QAM-256.

of the constellation diagrams implemented in the proposed concept for QAM-16, QAM-64 and QAM-256 respectively are represented in Fig. 3 and Fig. 4 [11]. In these examples the points are equally spaced, so the implementation of a grid on the axes will help for the correct positioning of the states. The more points in the constellation they are, the smaller the grid size Δ becomes. For the same dynamic range for the different QAMs (same maximum depth of the amplitude modulation on both axes) the axes are divided in one Δ-steps from -3Δ to +3Δ for QAM-16, from -7Δ to +7Δ for QAM-64 and from -15Δ to +15Δ for QAM-256. Above the points of the constellations the bit combinations they represent are given. In the case of the QAM-256 constellation diagram the bit patterns corresponding to the symbols are given in their decimal notation due to space constrains. It should be mentioned that there is an easy way to obtain the states for the three other quadrants from the first one quadrant symbols. This simple method involves the change of the two most significant bits from 00 to 10 to 11 to 01 rotating the diagram counterclockwise – the other least significant bits associated with the corresponding symbols remain the same. The remapping process will use a look-up table in the PM (Program Memory) of the DSP consisting of coordinate pairs (for the I- and Q-axes), evaluated for every data point in every implemented constellation diagram. After look-up of the data to be send both I- and Q-values in 12-bit representation (the

DACs resolution) are supplied via the interface to the modulator digital-to-analog converters.

V. Hardware implementation of the Digital Modulator – the DM9753 evaluation board

The detailed schematic diagram of the digital modulator board is given in Fig. 5. The two header ports for interconnecting the board with the digital signal processor evaluation system are JP1 (connected to SHARC EZ-KIT LITE connector J6) and JP2 (connected to SHARC EZ-KIT LITE connector J1). The pinout of the ports is the same as on the EZ-KIT LITE board, so a normal straight through ribbon cable (two of them) are the easiest way to connect the two boards. As will be shown later in the device prototype section photos there is a tendency to arrange the two boards in a way that two of the ports are near face to face and a very short length ribbon cable could be used to connect them, the other two being connected by a much longer cable. The use of equal length ribbon cables although not providing a compact look of the design is advisable, as one of the connectors carries the clock signal for the DACs (EXP_CLK) and part of the data bus signals (DATA42 – DATA47), while the other one carries the rest of the data bus signals (DATA0 – DATA41). Therefore if no displace and skew of clock to data should occur (resulting in word errors at the high transfer rates involved), then the transmission paths for the both port signals should be equal length.

As the converters U1 and U2 (AD9753) are 3.3V parts the manufacturer specification suggests a voltage translation when supplying them with 5V logic data. The inclusion of dedicated voltage translation integrated circuits for 48 data lines seems to be unnecessary and costly in terms of PCB space, therefore 48 voltage divider circuits are provided, consisting of resistors R24-R47, R48-R71, R72-R95 and R96-R119. The high data transfer rates (40MHz clocking for the 48-bit words) lead to degraded voltage slopes due to parasitic capacitances with standard suggested divider values of 1k and 1k8. Therefore this precaution measure is left to the cases where slower data update rates (lower MSymbol/sec rates) are involved and resistors R24-R47 and R72-R95 are omitted. For the same reason the serial resistors R48-R71 and R96-R119 are replaced with 100Ω values. This has done no harm to the DACs despite the different logic voltage levels used, so it proves to be a good solution.

The Digital-to-Analog Converters used (AD9753 [8]) are 12-bit fast (300MSPS) devices, so updating them with a 40MHz clock frequency (which leads to 80MSPS update rate) fits perfectly into their usable range leaving space for even faster modulators implementing more powerful signal processors. The DACs are designed for differential clock drive, but a single-ended clock interface is also possible as the implemented in the proposed design. It is achieved through the threshold setting divider networks R16-R17 and R18-R19 with the capacitors C16 and C17 providing filtering of the threshold voltage. The 40MHz clock signal, which is actually a buffered version of the EZ-KIT LITE system clock, is supplied to both converters through the serial resistors R20 and R21, which should limit overshot and ringing problems. A possible (but not implemented) voltage translation of the clock signal can be achieved through the R120-R121 divider. On the prototype board the R120 has been replaced with a 100Ω value and R121 is left unpopulated. There is an option to supply the clock to the DACs not from the EXP_CLK input but from the external memory write signal (WR\) through the R125 resistor. If this option is not used (as in the design proposed) R125 should be left unpopulated. The AD9753 employs an interesting architecture, where two consecutive samples data is supplied on two ports (every x 12-bit) of the converter (P1B11-P1B0 and P2B11-P2B0) and this 2x data is clocked into the DAC with a single clock source on a single clock cycle. This special feature is possible through the use of an internal PLL, doubling the external clock frequency. For the design proposed this means that clocking the converter with 40MHz actually leads to 80MHz conversion rate. The drawback is that 48-bit data is needed for supplying 4 12-bit values for 2 QAM symbols every cycle. This is a heavy computational burden for the DSP, so Direct Memory Access (DMA) will be implemented to transfer data. To accommodate different input clock rates the PLL range controller is set-up through the DIV1 and DIV0 logic levels (in the proposed design it is set to the range 25MHz – 100MHz). The PLL uses external loop filters (R22-C20 and R23-C21). The external PLL Reset input (RESET pin on U1 and U2) is implemented only in the PLL disabled mode to ensure proper synchronization, so in the 2x-clock-case it is tied to ground. The converter outputs are differential current type, so the full-scale current output is set through the resistors R14 and R15 connected to the FSADJ-pins. This maximum current is determined by the internal voltage reference (1.2V), divided by the current-setting resistor (1.9k) and amplified 32-times to give 20mA of driving capability. The internal reference needs to be carefully filtered, which is accomplished with the C18 and C19 capacitors. The

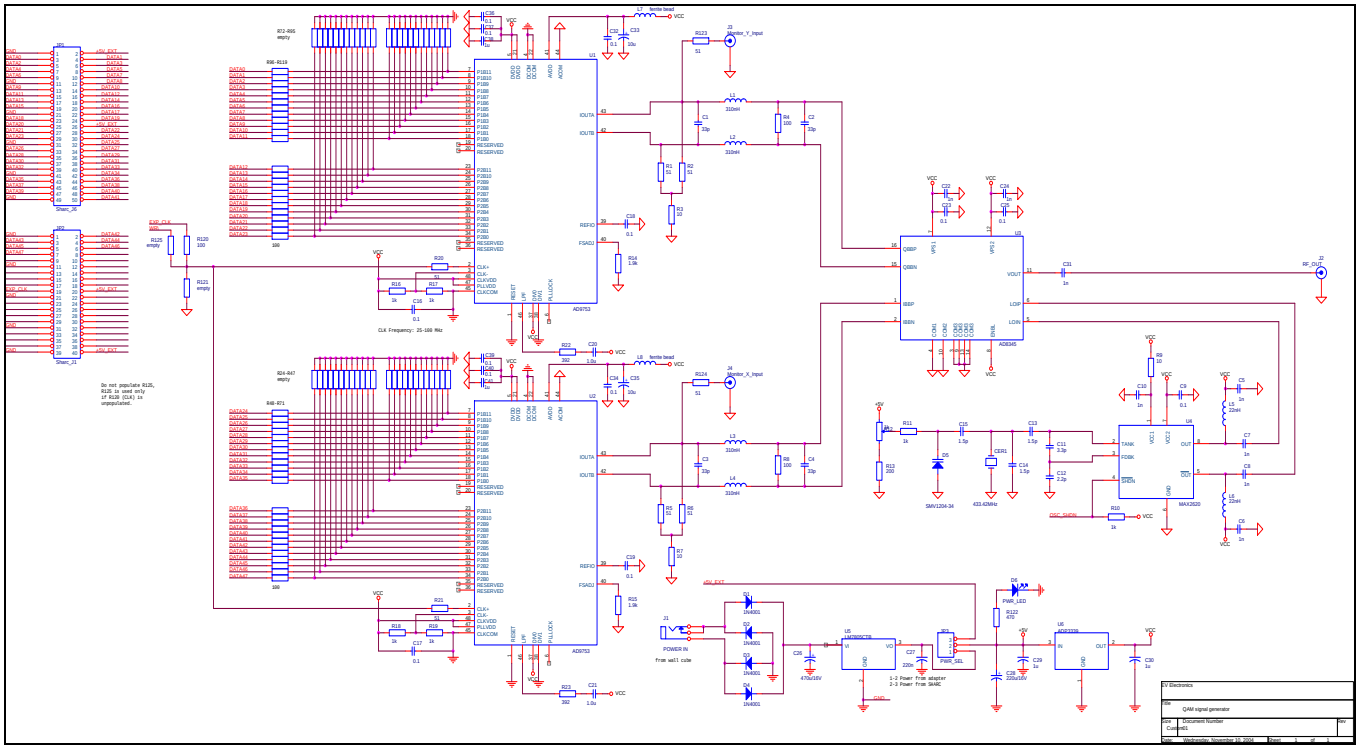

Fig.5. Complete schematics of the DM9753 digital modulator board (DSP-board not included).

two outputs IOUTA and IOUTB both swing between 0mA and 20mA. The composite load seen by them due to the filtering network and the I-to-V translating resistors R1, R2, R3, R5, R6 and R7 is 48Ω. Actually the full-scale differential voltage swing at the output should be $2V_{p\text{-}p}$, but it is limited to $1V_{p\text{-}p}$ at the inputs of the U3 modulator because the output resistors are not ground referenced but interconnected through the filtering network. The filter consisting of C1, L1, L2, R4 and C2 for the Q-channel and C3, L3, L4, R8 and C4 for the I-channel is a 51MHz low-pass filter. The separate analog and digital supply voltages of the digital-to-analog converters are carefully filtered by means of the C32-C41 and L7, L8 components. As monitoring the outputs of the DACs is the easiest way to observe the constellation diagrams of different digital modulations on a conventional oscilloscope, set in X-Y mode of operation, the monitoring points J3 and J4 with matching resistors R123 and R124 are provided. In an experimental setup the Y-input of the scope is connected to the J3 connector and the X-input is connected to the J4 connector.

The modulation of the QAM-data on a carrier is performed by the U3 AD8345 quadrature modulator [5]. This circuit has differential baseband inputs for the two component signals (I and Q), which should be biased to 0.7V and driven to a maximum $1.2V_{p\text{-}p}$ differential voltage. With such an arrangement (which is exactly followed by the proposed circuit) an output power of approximately -1dBm should be obtainable from the RF-output of the modulator (available at the J2 RF_OUT connector with AC decoupling accomplished by C31). The modulator is supplied with a differential LO (local oscillator) signal on its LOIP and LOIN-inputs, which should be AC-coupled to the external oscillator. This has been done with the C7 and C8 serial capacitors. The AD8345 internally generates its in-phase and quadrature LO-signals through a special phase splitter. This is the internal component which limits the usable frequency range of the carrier to 250MHz ÷ 1000MHz. Again the two power supplies of the modulator – one for the bias cell and the LO-buffers (VPS1) and one for the baseband voltage-to-current converters and the mixer core (VPS2), should be properly filtered, which is accomplished with the C22-C25 components. The AD8345 has an enable-pin, which can be used to put the device in power-saving sleep mode. This option is not used so the ENBL-pin is tied to the VCC-supply voltage.

The RF local oscillator signal at 433.92MHz is generated by the MAX2620 (U4) integrated oscillator with buffered outputs [9]. The part is perfectly suited to interface with the AD8345 as it has differential outputs. As these outputs are open-collector type they need external pull-ups. These pull-ups can be simple resistive matching networks (typically 50Ω), but optimal output power transfer is achieved when using

inductors as pull-ups and matching impedances simultaneously. This is the intention of including the L5 and L6 parts with additional power supply filtering components C5 and C6. The main building block of the MAX2620 is a common-collector negative resistance type oscillator, which employs parasitic elements in the IC to create the negative resistance at the base-emitter ports. The oscillation frequency is determined by an external resonant circuit, which can be both inductor and ceramic resonator. In the proposed design CER1 is the resonant tank, which is capacitively coupled to the oscillator, as it is internally biased to an optimal operating point. The coupling is accomplished through the C13 capacitor and both C11 and C12 components are used to fine-tune the negative resistance of the circuit for the desired frequency range. Depending on the type of the resonator tank circuit varying the C14 capacitor from 1.5pF to nearly 100pF in combination with long inductive leads will ease start of the oscillation. It is possible to fine-tune the frequency of the oscillation through the capacitively coupled (via C15) D5 varactor diode and the tuning components R11-R13. To increase the tuning range the tuning voltage is derived from the +5V supply and not from the down-regulated 3V3 needed for the integrated circuits. The MAX2620 can be shutdown through the SHDN\-pin, a feature that although not employed by this design (the SHDN\ is hardwired to the supply via R10 thus the part is always on) can be very useful in preventing EMC pollution and problems. As with the other integrated circuits on board proper filtering of the supply voltages is essential especially for achieving low noise and spurious performance of the oscillator. The R9, C9 and C10 components aid to achieve this design goal.

All integrated circuits in the design are powered by a 3.3V regulated power supply produced by the U6 ADP3339-3.3V integrated regulator [12]. Associated with this regulator are the filtering components C28-C30. There are two ways of obtaining the input voltage for the 3.3V regulator. The more conservative one is to use another +5V voltage regulator (U5 – LM7805) with its associated filtering components C26 and C27. The power for this on-board 5V regulator is obtained from a wall-cube adapter through the J1 power jack and the voltage reversal protecting diode bridge D1-D4. The other more compact solution is to derive the power for the DM9753 on-board regulator from the SHARC EZ-KIT LITE board. The advantage of this solution is its compactness as the external +5V is carried through the board interconnecting ribbon cables – the 5V line (+5V _EXT) and the ground (GND) are severely duplicated on the connectors JP1 and JP2. The selection between external wall-cube supply and SHARC derived power is done through a jumper setting at JP3 connector.

Fig.6. Component side of the DM9753 prototype board.

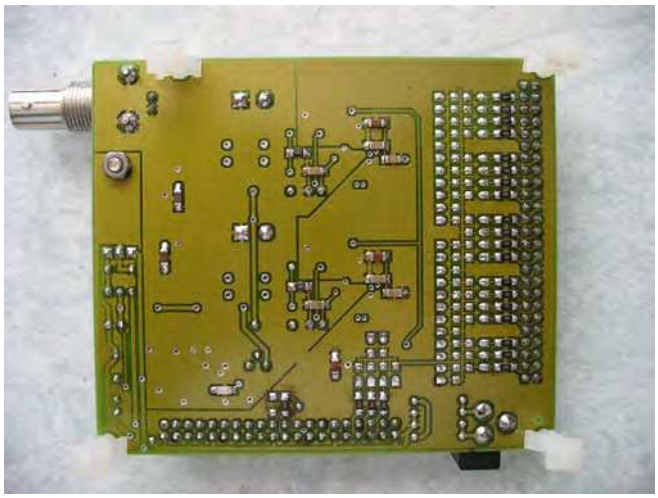

Fig.7. Solder side of the DM9753 prototype board.

VI. Device Prototype

The proposed DM9753 digital modulator board is a substantiation of the general concept of using a DSP to accomplish digital modulation. It was build as a daughter board to interface to the SHARC DSP EZ-KIT LITE evaluation board. Almost all parts on the PCB, which is a double-sided plated through holes type, are surface mounted devices. Photos of the prototype board are shown in Fig. 6 – Fig. 9. The top side of the board is presented in Fig. 6 and the bottom side in Fig. 7. The bottom side is very sparsely populated with components. The DSP-board with the ADSP-21061 SHARC processor is shown on the photo in Fig. 8 (the FLAG1 and IRQ1-buttons, which will be used to control the modulator, are visible) [6].

The complete assembly representing the digital modulator is shown on the photo in Fig. 9. The interconnecting ribbon cables of equal length, mentioned in the hardware implementation section, and the two scope probes connected at the QAM_X and QAM_Y outputs of the DM9753 used to display the QAM constellation diagrams on a conventional oscilloscope shall be noted.

Fig.8. The EZ-KIT LITE DSP evaluation board.

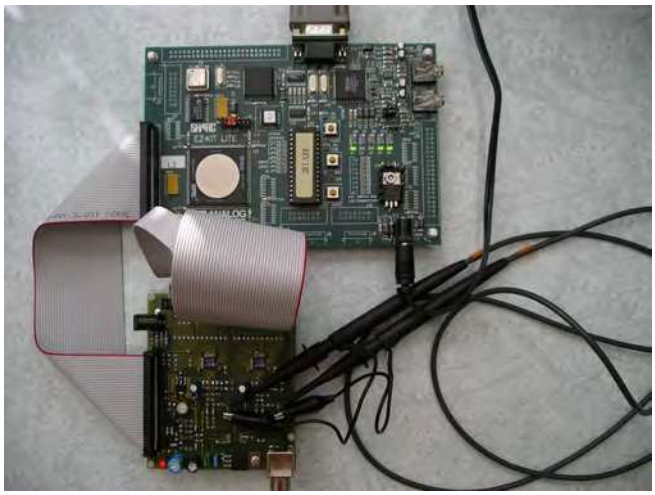

Fig.9. The complete digital modulator combining the DSP and DM9753 prototype boards.

VII. Conclusion

The proposed concept of a digital QAM modulator based on DSP-techniques and the practical implementation as the DM9753 evaluation prototype board presented in this article will be used in a future work to test various DSP-algorithms for performing different concomitant to the modulation tasks – symbol remapping, TCM-encoding, RRC-encoding to combat ISI, adding noise to random test sequences. The DSP-algorithms shall be tested on the prototype hardware implementation to prove the efficiency of the underlying concept.

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Received on: 26.01.2015